WHAT IS CLAIMED IS:

1. A processor comprising:

a CPU;

an instruction memory for storing a program; and

an invalid branch detection unit,

wherein when a branch instruction that changes an operation mode to another operation mode is executed by the program stored in the instruction memory, the invalid branch detection unit determines whether there is a branch enable instruction in a branch destination address, and in the presence of the branch enable instruction, the invalid branch detection unit permits a change in operation mode, while in the absence of the branch enable instruction, the invalid branch detection unit outputs an invalid branch detection signal.

2. The processor according to claim 1, further comprising:

an execution area judgment unit that judges an execution area from a value of a program counter of an instruction executed by the CPU;

an executive operation mode decision unit that decides an executive operation mode in accordance with the judgment of the execution area judgment unit;

a branch destination area judgment unit that judges a branch destination area from a value of a branch destination address when a branch instruction is executed by the program stored in the instruction memory;

a branch destination operation mode decision unit that decides a branch destination operation mode in accordance with the judgment of the branch destination area judgment unit; and

an operation mode change detection unit that detects a change in operation mode by comparing the executive operation mode decided by the executive operation mode decision unit with the branch destination operation mode decided by the branch destination operation mode decision unit,

wherein when a branch instruction is executed by the program stored in the instruction memory while there is not a branch enable instruction in the branch destination address, the invalid branch detection unit outputs the invalid branch detection signal on condition that the

operation mode change detection unit detects a change in operation mode.

3. The processor according to claim 2, wherein when a branch instruction is executed by the program stored in the instruction memory while there is not a branch enable instruction in the branch destination address, the invalid branch detection unit outputs the invalid branch detection signal on condition that the operation mode change detection unit detects a change in operation mode, and the change in operation mode detected by the operation mode detection unit does not coincide with any change in operation mode specified by the branch enable instruction.

4. The processor according to claim 1, wherein a specific instruction code that does not coincide with any other instructions is assigned to the branch enable instruction.

5. The processor according to claim 1, wherein an instruction code that corresponds to at least one of other instructions is assigned to the branch enable instruction.

6. The processor according to claims 3, further comprising a branch enable instruction code conversion unit that converts the instruction code of a branch enable instruction into an instruction code that corresponds to other instructions by detecting the branch enable instruction.

7. The processor according to claim 1, further comprising an interrupt output unit that outputs an interrupt request to the CPU by detecting the invalid branch detection signal output from the invalid branch detection unit.

8. The processor according to claim 1, further comprising a reset output unit that outputs a reset signal to the CPU by detecting the invalid branch detection signal output from the invalid branch detection unit.

9. The processor according to claim 1, further comprising an instruction conversion unit that converts an instruction in a branch destination address into an undefined instruction by detecting the invalid branch detection signal output from the invalid branch detection unit.

10. A compiler for creating a program for the processor according to any one of claims 1 to 9,

wherein when a source program is compiled into an assembler, the compiler inserts the branch enable instruction in a predetermined position of a program in a supervisor area by determining a function structure and an operation mode in the source program.